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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,577	12/04/2003	Chen-Jung Tsai	0941-0874P	5109

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,577	TSAI ET AL.	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Shim et al. (US 2004/0061202 A1)

In re claim 1, Shim (esp. Fig. 1) discloses a dual chips stacked packaging structure, comprising:

a first chip (26), having an active surface and an opposing non-active surface, the active surface consisting of a central area and peripheral area having a plurality of first bonding pads;

a lead frame (18), comprising a plurality of leads and a chip paddle (15) having a first adhering surface (at resin 28) and second adhering surface (at resin 32), the first adhering surface adhered the active surface of the first chip in such way to avoid contact with the first bonding pads;

a second chip (30), having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, the active surface consisting of a central area and a peripheral area having a plurality of second bonding pads; and

a plurality of wires (34, 36), wherein parts of the wires electrically connect with the first bonding pad and the leads, and parts of the wires electrically connect with the second bonding pad and the leads.

In re claim 2, Shim discloses the device of claim 1, wherein the first adhering surface of the chip paddle and the active surface of the first chip are adhered by a non-conductive solid or liquid adhesive[1].

In re claim 3, Shim discloses the device of claim 1, wherein the second adhering surface of the chip paddle and the non-active surface of the second chip are connected by a solid or liquid adhesive (resin 32).

In re claim 4, Shim discloses the device of claim 1, wherein the wires are metal lines.

In re claim 5, Shim (esp. Fig. 1) discloses a dual chips stacked packaging structure, comprising:

a first chip (26), having an active surface and an opposing non-active surface, the active surface consisting of a central area and peripheral area having a plurality of first bonding pads;

a lead frame (18), comprising a plurality of leads and a chip paddle (15) having a first adhering surface (at resin 28) and second adhering surface (at resin 32), the first adhering surface adhered the active surface of the first chip in such way to avoid contact with the first bonding pads;

a second chip (30), having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, the active surface consisting of a central area and a peripheral area having a plurality of second bonding pads; and

a plurality of wires (34, 36), wherein parts of the wires electrically connect with the first bonding pad and the leads, and parts of the wires electrically connect with the second bonding pad and the leads; and

an encapsulation (40) covering the lead frame, the first chip, the second chip and the wires.

In re claim 6, Shim discloses the device of claim 5, wherein each lead further comprises an inner lead covered by the encapsulation and outer lead extending beyond the encapsulation.

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[1] Note that Shim discloses this layer to comprise a "resin" but does not expressly disclose the conductive properties of the resin. That an epoxy resin such as used by Shim is insulative is well known in the prior art as taught by Oda et al. (U.S. Patent No. 6,489,668 B1; column 5, lines 23-30).

In re claim 7, Shim discloses the device of claim 5, wherein the first adhering surface of the chip paddle and the active surface of the first chip are adhered by a non-conductive solid or liquid adhesive[2].

In re claim 8, Shim discloses the device of claim 5, wherein the second adhering surface of the chip paddle and the non-active surface of the second chip are connected by a solid or liquid adhesive (resin 32).

In re claim 9, Shim discloses the device of claim 5, wherein the wires are metal lines.

In re claim 10, Shim (esp. Fig. 1) discloses a dual chips stacked packaging structure, comprising:

a first chip (26), having an active surface and an opposing non-active surface, the active surface consisting of a central area and peripheral area having a plurality of first bonding pads;

a lead frame (18), comprising a plurality of leads and a chip paddle (15) having a first adhering surface (at resin 28) and second adhering surface (at resin 32), the first adhering surface adhered the active surface of the first chip in such way to avoid contact with the first bonding pads;

a second chip (30), having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, the active surface consisting of a central area and a peripheral area having a plurality of second bonding pads; and

a plurality of wires (34, 36), wherein parts of the wires electrically connect with the first bonding pad and the leads, and parts of the wires electrically connect with the second bonding pad and the leads; and

[2] Note that Shim discloses this layer to comprise a "resin" but does not expressly disclose the conductive properties

an encapsulation (40) covering the chip paddle, the second chip, the wire connecting surface of the leads, the active surface of the first chip, and the wires, with the non-active surface of the first chip and the wire non-connecting surface of the leads exposed beyond the encapsulation.

In re claim 11, Shim discloses the device of claim 10, wherein each lead (18) further comprises an inner lead (20) covered by the encapsulation and outer lead extending beyond the encapsulation.

In re claim 12, Shim discloses the device of claim 10, wherein the first adhering surface of the chip paddle and the active surface of the first chip are adhered by a non-conductive solid or liquid adhesive[3].

In re claim 13, Shim discloses the device of claim 10, wherein the second adhering surface of the chip paddle and the non-active surface of the second chip are connected by a solid or liquid adhesive (resin 32).

In re claim 14, Shim discloses the device of claim 10, wherein the wires are metal lines.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

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of the resin. That an epoxy resin such as used by Shim is insulative is well known in the prior art as taught by Oda et al. (U.S. Patent No. 6,489,668 B1; column 5, lines 23-30).

[3] Note that Shim discloses this layer to comprise a "resin" but does not expressly disclose the conductive properties of the resin. That an epoxy resin such as used by Shim is insulative is well known in the prior art as taught by Oda et al. (U.S. Patent No. 6,489,668 B1; column 5, lines 23-30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815